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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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PHILIPS INTELLECTUAL PROPERTY & STANDARDS			RAINEY, ROBERT R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,605	STEER, WILLIAM A	
	Examiner	Art Unit	
	ROBERT R. RAINY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 20 May 2008.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7,9-14,16 and 17 is/are rejected.
 7) Claim(s) 8 and 15 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 14 April 2005 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 5/20/2008 with respect to the rejection of claims 1 and 10 under 35 U.S. C. §103 have been fully considered and were found to include both not persuasive and persuasive elements. Both are addressed below and new grounds of rejection are entered.

Applicant's argument that Akimoto does not teach a stepped voltage waveform being voltage-shifted by a capacitor is not persuasive. Applicant attacks the embodiments individually but it is the combination not the individual embodiments that were cited as teaching the elements. In addition, all embodiments of Akimoto include storing a voltage on the capacitor during a writing period and then applying a ramped or stepped voltage to the capacitor that is then voltage-shifted by the stored voltage. The fact that Akimoto does not use the term "voltage-shifted" does not negate the fact that the claimed feature is taught. For further explanation of the writing and driving cycles see for example the description given for embodiment 1 (for example at 6:11-7:6) to which both embodiments 3 and 6 refer to cover common features. And as in the rejection, examiner refers applicant to Fig. 13 with the further explanation that the stepped voltage applied to the left node of capacitor 82 during the driving phase will be voltage-shifted by the voltage stored on capacitor 82 during the writing phase so that the voltage at the gate of transistor 91 during the driving phase will be the applied step voltage plus the stored voltage.

Applicant's argument that examiner erred in applying *in re Boesch* to make a case for the obviousness of the step size being greater than the width of the linear operating region of the drive transistor is persuasive. Upon further review of Akimoto, examiner finds that Akimoto does teach this limitation. The mapping of Akimoto to the claimed limitation can be found in the new rejection below.

2. The amendments to claims 1, 4-10 and 14-17 effectively overcome the objections to these claims in the previous office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 1-7, 9-14 and 16-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,876,345 to *Akimoto et al.* ("Akimoto").

As to **claim 1**, *Akimoto* sixth embodiment discloses an active matrix electroluminescent display device comprising an array of display pixels (see for example column 5 lines 5-10 and column 1 lines 36-42), each pixel comprising: an electroluminescent display element (see for example Fig. 13 item 84 and

column 12 line 35) and ; a drive transistor (see for example Fig. 13 item 91 and column 12 lines 30-36) for driving a current through the display element, a drive voltage being provided to the gate of the drive transistor (see for example Fig. 3 and column 5 lines 40-42, which generally teaches to Vin to Vout relationship); and a storage capacitor (see for example Fig. 13 item 82 and column 12 lines 25-30) for storing a drive level (see for example "signal voltage" of Fig. 14 and column 12 lines 51-55) and connected between an input to the pixel and the gate of the drive transistor (see for example Fig. 13, which shows capacitor 82 so connected), wherein driver circuitry is provided for providing a linear voltage waveform to the input of the pixel (see for example Fig. 14 "PIXEL DRIVING VOLTAGE" associated with "DRIVING SIGNAL LINE" and column 12 lines 55-60), the voltage waveform being voltage-shifted by the storage capacitor before application to the gate of the drive transistor (see for example Fig. 13 and column 12 lines 51-60, which describe the storage of a signal voltage on the capacitor followed by the application of a triangular waveform to the capacitor through line 96; this results in the triangular waveform being voltage-shifted by the amount of the stored signal voltage before being applied to the gate of the drive transistor).

Akimoto sixth embodiment does not expressly disclose that the voltage waveform is stepped or that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor.

Akimoto third embodiment discloses that the voltage waveform is stepped and that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter and thus the drive transistor, i.e. item 31 or 32 of Fig. 6, is off at one step and on at another, and further that setting the writing signal at a medium level ensures that the switch point, i.e. linear operating region, is crossed in the transition from one step to another).

Akimoto sixth embodiment and *Akimoto* third embodiment are analogous art because they are from the same field of endeavor, which is image displays capable of multilevel display, and seek to solve the same problem, which is to reduce the variation in PWM circuits caused by differences between TFT circuitry.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the stepped waveform of *Akimoto* third embodiment to the circuit of *Akimoto* sixth embodiment. The suggestion/motivation would have been to provide advantages such as to prevent changes caused by noise (see for example column 10 lines 11-14).

As to **claim 2**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third embodiment further discloses that the height of the steps in the stepped voltage waveform is

sufficient to include the linear operating region voltages of the drive transistors of all pixels of the display (ibid. note that fig. 10 is representative of all pixels and thus applies to all drive transistors).

As to **claim 3**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third embodiment further discloses that the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the voltage applied to the gate of the drive transistor (ibid. note that Fig. 10 shows two different stored levels and that each of these is set at a midpoint between step levels; further see for example 10:15-21).

As to **claim 4**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third embodiment further discloses that each pixel further comprises an address transistor, connected between a power supply line and the gate of the drive transistor (see for example Fig. 13 item 89), and *Akimoto* third embodiment further discloses that each pixel further comprises an address transistor, connected between a power supply line and the gate of the drive transistor (see for example Fig. 6 item 9).

As to **claim 5**, in addition to the rejection of claim 4 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third and sixth embodiments further disclose means for disabling the driving of current by the drive transistor through the display element (see for example Fig. 5 noting that there is an “ILLUMINATING PERIOD” during which current driving of current through the display element is enabled and that during the rest of the driving period the driving of current by the drive transistor is disabled).

As to **claim 6**, in addition to the rejection of claim 5 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third and sixth embodiments disclose the claimed invention except for an isolating transistor in series with the drive transistor and the display element. It would have been obvious to one having ordinary skill in the art at the time the invention was made to add an additional transistor in series with the drive transistor of *Akimoto*, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8. In this case the two transistors would be driven on and off at the same time for example in order to reduce off state leakage current.

As to **claim 7**, in addition to the rejection of claim 4 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third and sixth embodiments further disclose disabling means comprising a switch for switching

the voltage on one terminal of the display elements of the array of pixels (see for example Fig. 13 item 89). To further prosecution examiner also notes that an power switch for the device would also read on the claim limitation as written.

As to **claim 9**, in addition to the rejection of claim 1 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* third and sixth embodiments further disclose that the device is operable to provide pulse width modulation (see for example 3:34-4:27; note that).

Akimoto third and sixth embodiments do not explicitly disclose the device is operable in at least two sequential phases, one phase providing coarse resolution pulse width modulation and the other, shorter phase, providing fine resolution pulse width modulation. However, since *Akimoto* does not confine the device to a single speed of operation it is reasonable to assume that it may be operated at two or more speeds, i.e. one faster and thus having shorter pulses or finer resolution. Since it is operable at two speeds it is operable in at least two sequential phases at the two different speeds. This could be accomplished for example by swapping oscillators or programming a different oscillation frequency.

Claim 10 claims the method implicit in the apparatus of claim 1 with the additional limitation that for a first set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned on, and for a second set of the

voltage steps applied to the gate of the drive transistor, the drive transistor is turned off, the first and second sets being determined by the stored pixel drive level and is rejected on the same grounds and arguments as claim 1 with the additional argument that Akimoto third embodiment teaches the additional limitation (see for example Fig. 10 and column 9 line 57 to column 10 line 21, noting that the inverter is on for period corresponding to a first set of steps indicated as being part of the “COLUMN ILLUMINATING PERIOD” and off for the rest or second set of steps).

The limitation of **claim 11** that the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor was covered by the rejection of claim 10 since this was a limitation included in claim 1.

As to **claim 12**, in addition to the rejection of claim 11 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, claims the method implicit in the apparatus of claim 2 and is rejected on the same grounds and arguments.

As to **claim 13**, in addition to the rejection of claim 10 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, claims the method implicit in the apparatus of claim 3 and is rejected on the same grounds and arguments.

As to **claim 14**, in addition to the rejection of claim 10 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, claims the method implicit in the apparatus of claim 8 and is rejected on the same grounds and arguments.

As to **claim 16**, in addition to the rejection of claim 10 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, claims the method implicit in the apparatus of claim 9 and is rejected on the same grounds and arguments.

As to **claim 17**, in addition to the rejection of claim 16 over *Akimoto* sixth embodiment and *Akimoto* third embodiment, *Akimoto* sixth and third embodiments further disclose that the stepped voltage waveform to the input of the pixel has the same voltage levels in the two phases, and the shorter phase has shorter step transitions (since the sequential use of *Akimoto* from claim 16 changed only the speed one can reasonably assume that the voltage steps would remain the same).

Allowable Subject Matter

3. Claims 8 and 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
4. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not disclose disabling the driving of current by the drive

transistor through the display element during the storing of a pixel drive level voltage on the storage capacitor in addition to the limitations of the claims from which claims 8 and 15 depend. Note that Akimoto in Fig. 17 and 18 shows as prior art a circuit described at Akimoto 1:43-2:39 that includes means for disabling the driving of current (Fig. 17 transistor 223) by the drive transistor through the display element during the storing of a pixel drive level voltage on the storage capacitor, but this prior art circuit is not taught as operating in a PWM manner from a stepped waveform with steps larger than the linear region of the drive transistors and the function of the circuit of Akimoto would be destroyed by the addition of an isolation transistor as shown in Akimoto Fig. 17 because the charging path for the capacitor during the writing phase would be lost.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/
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